



Contrast Enhancer v1.0

Product Brief

Introduction

Contrast Enhancer IP Core is a video processing IP core used to enhance the contrast of input video stream. Contrast control is provided in all modern video processing systems to improve viewing comfort. Contrast is a major determinant of perceived picture quality.

Contrast control IP core helps system designers who build miniature FPGA based video processing systems to implement the feature with minimum extra effort. The algorithm runs in RGB domain and enables the designer to tune Red, Green and Blue contrast values separately. The IP core is fully verified in ModelSim environment and validated in real hardware.

The architecture takes advantage of high-performance XtremeDSP slices available in Xilinx Virtex 5 FPGA.

Features

- Real time video processing
- Support for RGB 8:8:8
- 256 programmable contrast steps
- Pixel by pixel processing
- Requires only a single clock input
- Support input resolution from QVGA to SXGA
- Optimized for Xilinx Virtex-5 FPGA

Applications

- Medical Endoscope
- Consumer Displays
- Video Surveillance
- Video Conferencing
- Machine Vision

Core Resource Utilization and Performance

Resource utilization after Place and Route in Virtex5 FPGA (XC5VSX50T-1FFG1136) is given in the table below.

Resource Type	Quantity Used
Slice Register	31
Slice LUT	79
Block RAM	0
DSP48E	3
Maximum Clock Frequency	350 MHz

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements using ModelSim and validated in Xilinx ML506 XtremeDSP development kit equipped with Virtex5 FPGA (XC5VSX50T-1FFG1136).

Standard Deliverables

- RTL source code in VHDL or post-synthesis EDIF/NGC netlist
- Sophisticated VHDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Product Datasheet
- Comprehensive User Guide with detailed application notes

Documentation

- Contrast Enhancer Datasheet
- Contrast Enhancer User Guide

Purchase and Technical Support

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